



CAT22C10

256-Bit Nonvolatile CMOS Static RAM

FEATURES

- Single 5V Supply
- Fast RAM Access Times:
 - 200ns
 - 300ns
- Infinite E²PROM to RAM Recall
- CMOS and TTL Compatible I/O
- Power Up/Down Protection
- 100,000 Program/Erase Cycles (E²PROM)
- Low CMOS Power Consumption:
 - Active: 40mA Max.
 - Standby: 30 μ A Max.
- JEDEC Standard Pinouts:
 - 18-pin DIP
 - 16-pin SOIC
- 10 Year Data Retention
- Commercial, Industrial and Automotive Temperature Ranges

DESCRIPTION

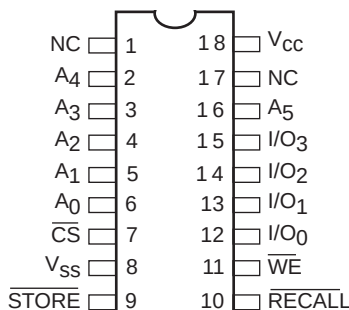
The CAT22C10 NVRAM is a 256-bit nonvolatile memory organized as 64 words x 4 bits. The high speed Static RAM array is bit for bit backed up by a nonvolatile E²PROM array which allows for easy transfer of data from RAM array to E²PROM (STORE) and from E²PROM to RAM (RECALL). STORE operations are completed in 10ms max. and RECALL operations typically within 1.5 μ s. The CAT22C10 features unlimited RAM write operations either through external RAM

writes or internal recalls from E²PROM. Internal false store protection circuitry prohibits STORE operations when V_{CC} is less than 3.0V.

The CAT22C10 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles (E²PROM) and has a data retention of 10 years. The device is available in JEDEC approved 18-pin plastic DIP and 16-pin SOIC packages.

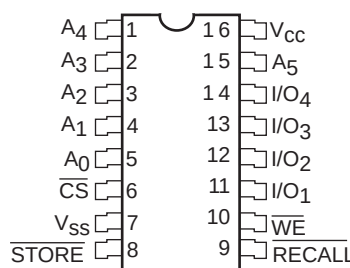
PIN CONFIGURATION

DIP Package (P)



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SOIC Package (J)

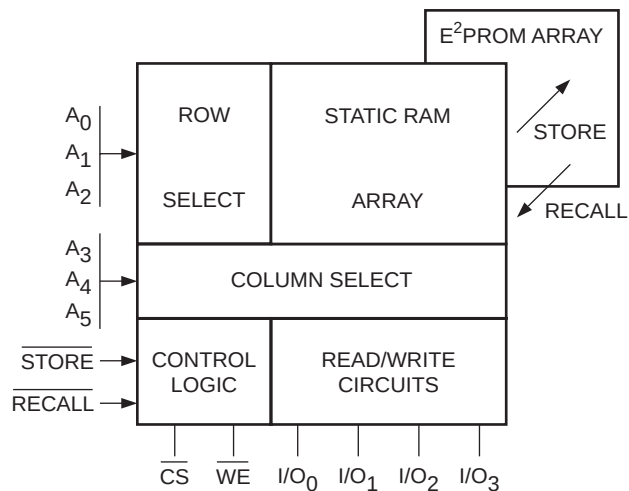


22C10 F02

PIN FUNCTIONS

Pin Name	Function
A ₀ –A ₅	Address
I/O ₀ –I/O ₃	Data In/Out
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CS}}$	Chip Select
$\overline{\text{RECALL}}$	Recall
$\overline{\text{STORE}}$	Store
V _{CC}	+5V
V _{SS}	Ground
NC	No Connect

BLOCK DIAGRAM



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MODE SELECTION⁽¹⁾⁽²⁾⁽³⁾

Mode	Input				I/O
	$\overline{CS}$	$\overline{WE}$	$\overline{RECALL}$	$\overline{STORE}$	
Standby	H	X	H	H	Output High-Z
RAM Read	L	H	H	H	Output Data
RAM Write	L	L	H	H	Input Data
(E ² PROM→RAM)	X	H	L	H	Output High-Z RECALL
(E ² PROM→RAM)	H	X	L	H	Output High-Z RECALL
(RAM→E ² PROM)	X	H	H	L	Output High-Z STORE
(RAM→E ² PROM)	H	X	H	L	Output High-Z STORE

POWER-UP TIMING⁽⁴⁾

Symbol	Parameter	Min.	Max.	Units
VCCSR	V _{CC} Slew Rate	0.5	0.005	V/ms

Note:

- (1) $\overline{RECALL}$ signal has priority over $\overline{STORE}$ signal when both are applied at the same time.
- (2) $\overline{STORE}$ is inhibited when $\overline{RECALL}$ is active.
- (3) The store operation is inhibited when V_{CC} is below ≈ 3.0V.
- (4) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground ⁽²⁾	-2.0 to +V _{CC} +2.0V
V _{CC} with Respect to Ground	-2.0V to +7.0V
Package Power Dissipation Capability (T _a = 25°C)	1.0W
Lead Soldering Temperature (10 secs)	300°C
Output Short Circuit Current ⁽³⁾	100 mA

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N _{END} ⁽¹⁾	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T _{DR} ⁽¹⁾	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V _{ZAP} ⁽¹⁾	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I _{LTH} ⁽¹⁾⁽⁴⁾	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.	Max.		
I _{CC}	Current Consumption (Operating)			40	mA	All Inputs = 5.5V T _A = 0°C All I/O's Open
I _{SB}	Current Consumption (Standby)			30	μA	$\overline{CS} = V_{CC}$ All I/O's Open
I _{LI}	Input Current			10	μA	0 ≤ V _{IN} ≤ 5.5V
I _{LO}	Output Leakage Current			10	μA	0 ≤ V _{OUT} ≤ 5.5V
V _{IH}	High Level Input Voltage	2		V _{CC}	V	
V _{IL}	Low Level Input Voltage	0		0.8	V	
V _{OH}	High Level Output Voltage	2.4			V	I _{OH} = -2mA
V _{OL}	Low Level Output Voltage			0.4	V	I _{OL} = 4.2mA
V _{DH}	RAM Data Holding Voltage	1.5		5.5	V	V _{CC}

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Unit	Conditions
C _{I/O} ⁽¹⁾	Input/Output Capacitance	10	pF	V _{I/O} = 0V
C _{IN} ⁽¹⁾	Input Capacitance	6	pF	V _{IN} = 0V

Note:

- (1) This parameter is tested initially and after a design or process change that affects the parameter.
- (2) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
- (3) Output shorted for no more than one second. No more than one output shorted at a time.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V_{CC} +1V.

A.C. CHARACTERISTICS, Write Cycle

$V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Symbol	Parameter	22C10-20		22C10-30		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	200		300		ns	$C_L = 100pF$ +1TTL gate $V_{OH} = 2.2V$ $V_{OL} = 0.65V$ $V_{IH} = 2.2V$ $V_{IL} = 0.65V$
t_{CW}	$\overline{CS}$ Write Pulse Width	150		150		ns	
t_{AS}	Address Setup Time	50		50		ns	
t_{WP}	Write Pulse Width	150		150		ns	
t_{WR}	Write Recovery Time	25		25		ns	
t_{DW}	Data Valid Time	100		100		ns	
t_{DH}	Data Hold Time	0		0		ns	
$t_{WZ}^{(1)}$	Output Disable Time		100		100	ns	
t_{OW}	Output Enable Time	0		0		ns	

A.C. CHARACTERISTICS, Read Cycle

$V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Symbol	Parameter	22C10-20		22C10-30		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	200		300		ns	$C_L = 100pF$ +1TTL gate $V_{OH} = 2.2V$ $V_{OL} = 0.65V$ $V_{IH} = 2.2V$ $V_{IL} = 0.65V$
t_{AA}	Address Access Time		200		300	ns	
t_{CO}	$\overline{CS}$ Access Time		200		300	ns	
t_{OH}	Output Data Hold Time	0		0		ns	
$t_{LZ}^{(1)}$	$\overline{CS}$ Enable Time	0		0		ns	
$t_{HZ}^{(1)}$	$\overline{CS}$ Disable Time		100		100	ns	

Note:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

A.C. CHARACTERISTICS, Store Cycle

$V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
t_{STC}	Store Time		10	ms	$C_L = 100\text{pF} + 1\text{TTL gate}$ $V_{OH} = 2.2\text{V}, V_{OL} = 0.65\text{V}$ $V_{IH} = 2.2\text{V}, V_{IL} = 0.65\text{V}$
t_{STP}	Store Pulse Width	200		ns	
$t_{STZ}^{(1)}$	Store Disable Time		100	ns	
$t_{OST}^{(1)}$	Store Enable Time	0		ns	

A.C. CHARACTERISTICS, Recall Cycle

$V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
t_{RCC}	Recall Cycle Time	1.4		μs	$C_L = 100\text{pF} + 1\text{TTL gate}$ $V_{OH} = 2.2\text{V}, V_{OL} = 0.65\text{V}$ $V_{IH} = 2.2\text{V}, V_{IL} = 0.65\text{V}$
t_{RCP}	Recall Pulse Width	300		ns	
t_{RCZ}	Recall Disable Time		100	ns	
t_{ORC}	Recall Enable Time	0		ns	
t_{ARC}	Recall Data Access Time		1.1	μs	

Note:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

DEVICE OPERATION

The configuration of the CAT22C10 allows a common address bus to be directly connected to the address inputs. Additionally, the Input/Output (I/O) pins can be directly connected to a common I/O bus if the bus has less than 1 TTL load and 100pF capacitance. If not, the I/O path should be buffered.

When the chip select ($\overline{CS}$) pin goes low, the device is activated. When $\overline{CS}$ is forced high, the device goes into the standby mode and consumes very little current. With the nonvolatile functions inhibited, the device operates like a Static RAM. The Write Enable ($\overline{WE}$) pin selects a write operation when $\overline{WE}$ is low and a read operation when $\overline{WE}$ is high. In either of these modes, an array byte (4 bits) can be addressed uniquely by using the address lines (A_0 – A_5), and that byte will be read or written to through the Input/Output pins (I/O_0 – I/O_3).

The nonvolatile functions are inhibited by holding the $\overline{STORE}$ input and the $\overline{RECALL}$ input high. When the $\overline{RECALL}$ input is taken low, it initiates a recall operation which transfers the contents of the entire E²PROM array

into the Static RAM. When the $\overline{STORE}$ input is taken low, it initiates a store operation which transfers the entire Static RAM array contents into the E²PROM array.

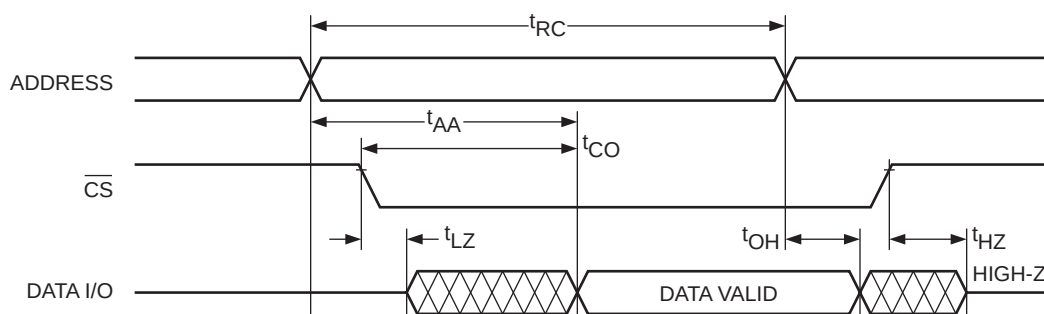
Standby Mode

The chip select ($\overline{CS}$) input controls all of the functions of the CAT22C10. When a high level is supplied to the $\overline{CS}$ pin, the device goes into the standby mode where the outputs are put into a high impedance state and the power consumption is drastically reduced. With I_{SB} less than 100 μ A in standby mode, the designer has the flexibility to use this part in battery operated systems.

Read

When the chip is enabled ($\overline{CS}$ = low), the nonvolatile functions are inhibited ($\overline{STORE}$ = high and $\overline{RECALL}$ = high). With the Write Enable ($\overline{WE}$) pin held high, the data in the Static RAM array may be accessed by selecting an address with input pins A_0 – A_5 . This will occur when the outputs are connected to a bus which is loaded by no more than 100pF and 1 TTL gate. If the loading is greater than this, some additional buffering circuitry is recommended.

Figure 1. Read Cycle Timing



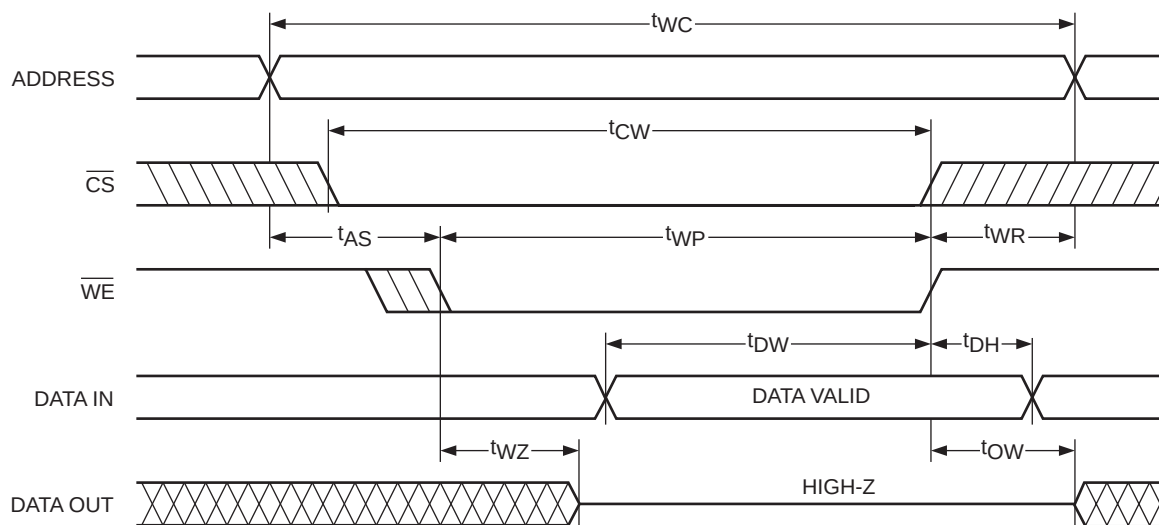
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Write

With the chip enabled and the nonvolatile functions inhibited, the Write Enable ($\overline{WE}$) pin will select the write mode when driven to a low level. In this mode, the address must be supplied for the byte being written. After the set-up time (t_{AS}), the input data must be supplied to pins I/O₀–I/O₃. When these conditions, in-

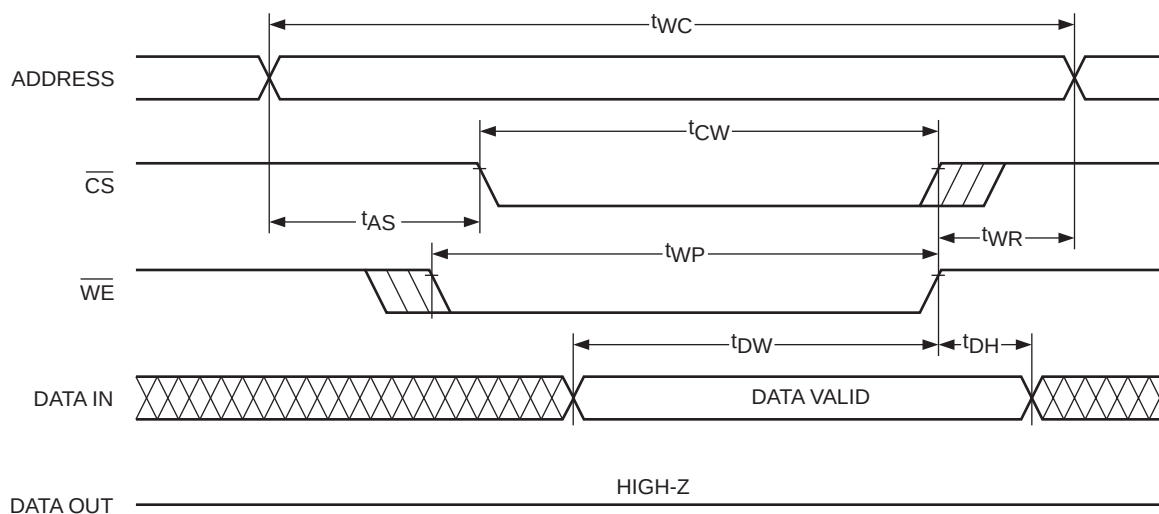
cluding the write pulse width time (t_{WP}) are met, the data will be written to the specified location in the Static RAM. A write function may also be initiated from the standby mode by driving $\overline{WE}$ low, inhibiting the nonvolatile functions, supplying valid addresses, and then taking $\overline{CS}$ low and supplying input data.

Figure 2. Write Cycle Timing



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Figure 3. Early Write Cycle Timing



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Recall

At any time, except during a store operation, taking the $\overline{\text{RECALL}}$ pin low will initiate a recall operation. This is independent of the state of $\overline{\text{CS}}$, $\overline{\text{WE}}$, or $\text{A}_0\text{--A}_5$. After the $\overline{\text{RECALL}}$ pin has been held low for the duration of the Recall Pulse Width (t_{RCP}), the recall will continue independent of any other inputs. During the recall, the entire contents of the E²PROM array is transferred to the Static RAM array. The first byte of data may be externally accessed after the recalled data access time from end of recall (t_{ARC}) is met. After this, any other byte may be accessed by using the normal read mode.

If the $\overline{\text{RECALL}}$ pin is held low for the entire Recall Cycle time (t_{RCC}), the contents of the Static RAM may be immediately accessed by using the normal read mode. A recall operation can be performed an unlimited number of times without affecting the integrity of the data.

The outputs $\text{I/O}_0\text{--I/O}_3$ will go into the high impedance state as long as the $\overline{\text{RECALL}}$ signal is held low.

Store

At any time, except during a recall operation, taking the $\overline{\text{STORE}}$ pin low will initiate a store operation. This takes

place independent of the state of $\overline{\text{CS}}$, $\overline{\text{WE}}$ or $\text{A}_0\text{--A}_5$. The $\overline{\text{STORE}}$ pin must be held low for the duration of the Store Pulse Width (t_{STP}) to ensure that a store operation is initiated. Once initiated, the $\overline{\text{STORE}}$ pin becomes a “Don’t Care”, and the store operation will complete its transfer of the entire contents of the Static RAM array into the E²PROM array within the Store Cycle time (t_{STC}). If a store operation is initiated during a write cycle, the contents of the addressed Static RAM byte and its corresponding byte in the E²PROM array will be unknown.

During the store operation, the outputs are in a high impedance state. A minimum of 100,000 store operations can be performed reliably and the data written into the E²PROM array has a minimum data retention time of 10 years.

DATA PROTECTION DURING POWER-UP AND POWER-DOWN

The CAT22C10 has on-chip circuitry which will prevent a store operation from occurring when V_{CC} falls below 3.0V typ. This function eliminates the potential hazard of spurious signals initiating a store operation when the system power is below 3.0V typ.

Figure 4. Recall Cycle Timing

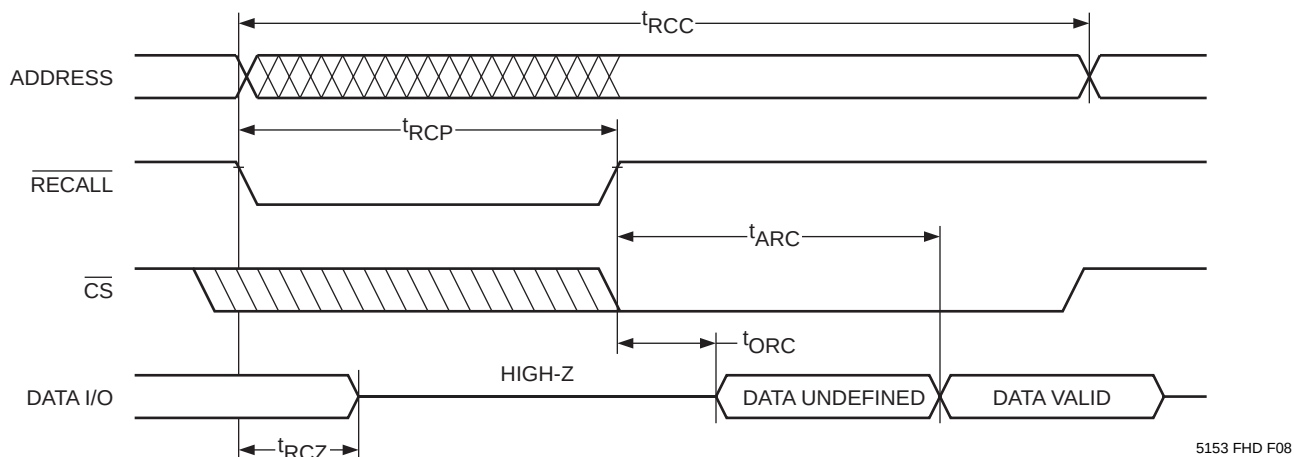
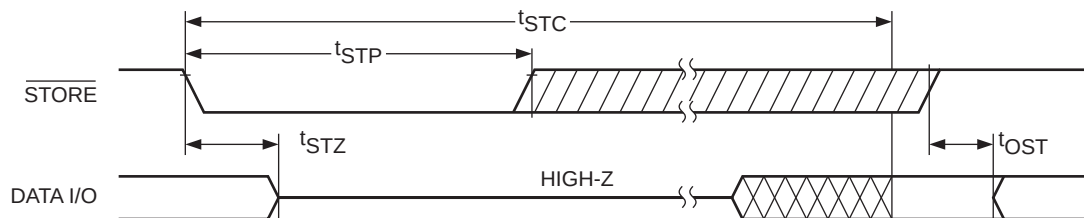
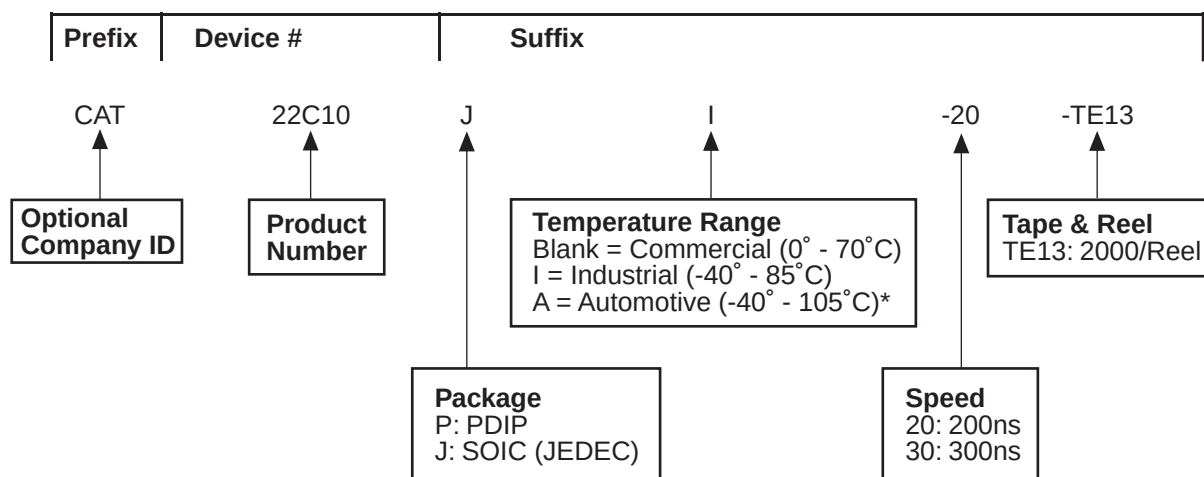


Figure 5. Store Cycle Timing



ORDERING INFORMATION



* -40° to +125°C is available upon request

22C10 F08

Notes:

(1) The device used in the above example is a 22C10JI-20TE13 (SOIC, Industrial Temperature, 200ns Access Time, Tape & Reel)

